Electronic Version
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UNIVERSAL TEST PLATFORM AND TEST METHOD FOR LATCH-UP

Abstract

A method for testing latch-up phenomenon of a chip is provided. The chip is tested on a test platform, the test platform storing a test program of the chip for testing the chip. The method includes (a) obtaining the test program of the chip tested on the test platform, (b) obtaining pin data of the chip by the test program of the chip, (c) setting up an input pin of the chip with an initial value, and (d) providing a test current to the pin of the chip, and then measuring the current between a power end and a ground end of the chip to see if it exceeds a first predetermined value.